

The opinion in support of the decision being entered today is *not* binding
precedent of the Board.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte ALAN FOLMSBEE

Appeal 2007-1836
Application 09/376,654
Technology Center 2100

Decided: August 30, 2007

Before JAMES D. THOMAS, KENNETH W. HAIRSTON, and
MAHSHID D. SAADAT, *Administrative Patent Judges*.

HAIRSTON, *Administrative Patent Judge*.

DECISION ON APPEAL

Appellant appeals under 35 U.S.C. § 134 from the Final Rejection of
claims 1, 3, 4, 13, 17, and 18. We have jurisdiction under 35 U.S.C. § 6(b).

We will affirm the indefiniteness rejection, and reverse the
anticipation rejection.

STATEMENT OF THE CASE

Appellant has invented a processor and a method for the same wherein errors in instructions are intentionally introduced to the processor. In response to the errors in the instructions, a programmable error correcting circuit generates corrected processor instructions that permit the processor to operate with the corrected processor instructions (Figures 1 and 11; Specification 3, 4, and 22).

Claim 1 is representative of the claims on appeal, and it reads as follows:

1. A particularly configurable processor for processing error induced computer programs which are selectively operable on said particularly configurable processor, comprising:

a central processing unit chip;

processor circuitry on said chip;

a programmable error correcting circuit on said chip;

RAM on said chip storing error correcting information, said RAM being in communication with said programmable error correcting circuit; and wherein:

the programmable error correcting circuit receives said error correcting information and processor instructions containing errors that are not capable of being executed by said processing circuitry, and

said programmable error correcting circuit generates corrected processor instructions in response to said processor instructions containing errors and said error correcting information, the corrected processor instructions being capable of being executed by said processing circuitry.

Appeal 2007-1836
Application 09/376,654

The prior art relied upon by the Examiner in rejecting the claims on appeal is:

Chen	U.S. 6,044,483	Mar. 28, 2000 (filed Jan. 29, 1998)
------	----------------	--

The Examiner rejected claim 4 under the second paragraph of 35 U.S.C. § 112 for indefiniteness. The Examiner rejected claims 1, 3, 4, 13, 17, and 18 under 35 U.S.C. § 102(e) based upon the teachings of Chen.

Appellant acknowledges that claim 4 is indefinite because the limitation “the error correction key” lacks antecedent basis (Br. 6).

Appellant contends *inter alia* that Chen mentions intentionally inserting an error in a corrected data word, but does not mention intentionally placing errors in instructions in a computer program loaded in a microprocessor, and then correcting the erroneous instructions via error correcting information (Br. 10; Reply Br. 7).

ISSUE

Does Chen introduce erroneous instructions into the computer system, and then correct the erroneous instructions for processing by the computer system?

FINDINGS OF FACT

Figures 1 and 11 of Appellant’s drawing show a CPU 11, 161 on a single chip that receives instructions with errors intentionally placed therein. The programmable error correcting circuitry 169 generates corrected processor instructions in response to the erroneous instructions, and the corrected instructions are executed by the processor.

Chen describes a method and apparatus for performing error detection and correction of single and multiple data bit errors (Figure 1; col. 4, ll. 30 to

Appeal 2007-1836
Application 09/376,654

41). The apparatus is on a dual in-line memory module (DIMM) card 101 along with one or more DRAM memory chips 102 which are all implemented within an application specific integrated circuit (ASIC) (col. 7, ll. 4 to 8). The ASIC chip interconnects data bus 104 with the memory chips 102 (col. 7, ll. 8 to 11). The data passing from the data bus 104 to the memory chips 102 and the data passing from the memory chips 102 to the data bus 104 undergoes error correction by error correcting code (ECC) logic 103 on the ASIC (col. 7, ll. 11 to 22). Chen specifically states that an intentional error that is readily detected and corrected is caused in an ECC data word that has undergone error correction via the ECC logic (col. 5, ll. 34 to 38; col. 25, ll. 35 to 41). The introduction of the intentional error serves as a notification to the system that an error has occurred, and to allow the implementation of various maintenance strategies (col. 5, ll. 38 to 43).

PRINCIPLE OF LAW

Anticipation is established when a single prior art reference discloses expressly or under the principles of inherency each and every limitation of the claimed invention. *Atlas Powder Co. v. IRECO Inc.*, 190 F.3d 1342, 1347, 51 USPQ2d 1943, 1946 (Fed. Cir. 1999); *In re Paulsen*, 30 F.3d 1475, 1478-79, 31 USPQ2d 1671, 1673 (Fed. Cir. 1994).

ANALYSIS

As indicated *supra*, Appellant acknowledges that claim 4 on appeal is indefinite.

Turning to the anticipation rejection, we agree with the Appellant that Chen intentionally places an error in a corrected data word, but does not

Appeal 2007-1836
Application 09/376,654

intentionally place an error in an instruction and then correct the same prior to processing by a processor as set forth in the claims on appeal.

CONCLUSION OF LAW

The indefiniteness of claim 4 has been demonstrated by the Examiner. Anticipation has not been established by the Examiner for claims 1, 3, 4, 13, 17, and 18 because Chen lacks a teaching of introduction of an instruction with errors into a processor, and correction of the erroneous instruction prior to processing by the processor.

DECISION

The indefiniteness rejection of claim 4 is affirmed. The anticipation rejection of claims 1, 3, 4, 13, 17, and 18 is reversed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED-IN-PART

rwk

MARTINE PENILLA & GENCARELLA, LLP
710 LAKEWAY DRIVE
SUITE 200
SUNNYVALE CA 94085